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PATENT

#5 IDS
3/7/02
V. Vannall

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Raaijmakers et al.	Group Art Unit 2812
App. No.	:	09/764,711	
Filed	:	January 18, 2001	
For	:	METHOD OF DEPOSITING SILICON WITH HIGH STEP COVERAGE	
Examiner	:	Roman, A.	

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Enclosed is form PTO-1449 listing 5 references that are also enclosed. This Information Disclosure Statement is being filed under 37 C.F.R. § 1.97(c)(2) before the mailing date of a final action and before the mailing of a Notice of Allowance. This Statement is accompanied by the fees set forth in 37 C.F.R. § 1.17(p). The Commissioner is hereby authorized to charge any additional fees which may be required or to credit any overpayment to Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: January 24, 2002

By: [signature]

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FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(USE SEVERAL SHEETS IF NECESSARY)

ATTY. DOCKET NO. ASMEX.186DV1

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APPLICATION NO. 09/764,711

APPLICANT Raaijmakers et al.

FILING DATE January 18, 2001

GROUP 2812

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

EXAMINER INITIAL		**OTHER DOCUMENTS** (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
		Coffa et al., "Defect Production and Annealing in Ion-Implanted Amorphous Silicon," Physical Review Letters, Vol. 70, No. 24, (June 14, 1993), pp.3756-3759.
		Kakkad et al., "Crystallized Si films by low-temperature rapid thermal annealing of amorphous silicon," J. Appl. Phys., Vol. 65, No. 5, (March 1, 1989), pp. 2069-2072.
		Lin et al., "Front-End Integration Effects On Gate Oxide Quality," Mat. Res. Soc. Symp. Proc., Vol. 428, (1996), pp. 361-366.
		Voutsas, "Low Temperature Polysilicon Technology for Advanced Display Systems," **Shapu Giho/Sharp Technical Journal,** No. 69, (December 1997), pp. 51-56.
		Wu, "Suppression of the Boron Penetration Induced Dielectric Degradation by Using a Stacked-Amorphous-Silicon Film as the Gate Structure for pMOSFET," IEEE Transactions On Electron Devices, Vol. 43, No. 2, (February 1996), pp. 303-310.

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EXAMINER	DATE CONSIDERED

*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED, INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.